REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Claim amendments are presented herein to obviate the current rejection. No new matter has been added.

35 USC § 112

Claim 15 has been amended to swap the phrase "central databases" with "central database".

35 USC § 101

Claims 1-25 stand rejected under 35 USC § 101. These rejections are respectfully traversed.

Claim 1 has been amended to recite "to generate a logic design as part of an electrical circuit". Claim 7 has been amended to recite "using the defined signal parameter that is maintained in the central database in computer code for a logic design forming part of an electrical circuit". Claim 15 recites "an interface between the central databases and a logic design module that uses the signal parameters in a logic design forming part of an electrical circuit". The generation of a part of an electric circuit as recited in the claims comprises a concrete, tangible, and useful result and also changes the logic design to

a different state. Hence, the claims defense subject matter for which a patent may be obtained. Accordingly, it is respectfully requested that the rejection of claims 1-17 under 35 USC § 101 be withdrawn.

Claim 18 has been amended to recite "A machine-accessible medium containing instructions which cause a machine to perform operations comprising:". Therefore, claim 18 is directed towards statutory subject matter. Accordingly, it is respectfully requested that the rejection of claims 18-25 under 35 USC § 101 be withdrawn.

35 USC § 103

Claims 1, 2, 5-8, 11-19, and 22-25 stand rejected under 35 USC § 103(a) as allegedly being unpatentable over ExpressiveSystems in view of Yamagishi. Claims 3, 4, 9, 10, 20, and 21 stand rejected under 35 USC § 103(a) as allegedly being unpatentable over ExpressiveSystems in view of Yamagishi and IEEEVerilog. These rejections are respectfully traversed.

Claim 1 has been amended to include features from previous claim 2 to recite "a logic design module operable to be used by one or more users to generate a logic design as part of an electrical circuit; and a central database integrated with the logic design module and including modifiable signal parameters that are accessible for use by the users of the logic design

module; wherein the logic design module is operable to automatically update the logic design when the signal parameters in the central database are modified."

Claim 7 has been amended to include features from previous claim 8 and to recite "defining a signal parameter with a value; maintaining the defined signal parameter in a central database; using the defined signal parameter that is maintained in the central database in computer code for a logic design forming part of an electrical circuit comprising a plurality of components; updating the value of the defined signal parameter in the central database; and automatically updating the logic design with the updated value of the defined signal parameter when the value of the defined signals is updated in the central database." Claim 18 contains similar features.

Claim 15 has been amended to recite "an interface between the central databases and a logic design module that uses the signal parameters in a logic design forming part of an electrical circuit; wherein the value for the defined signal parameters in the central database is operable to be modified; and wherein the logic design is automatically updated with the modified value of the defined signal parameters when the value for the defined signal parameters in the central database is modified."

Neither of ExpressiveSystems and Yamagishi contemplate an arrangement in which a logic design may be automatically updated based on modifications to signal parameters as defined in the claims. ExpressiveSystems on pages 23-25 illustrates a configuration in which the activation of a graphical user interface element entitled connect causes port 1 to be connected to block 1. As a part of this connection, a Net Editor window is provided in which free signals in port 1, block 1, and on net may be established. Thereafter, the design of this connection may be saved and associated code generated.

Yamagishi describes an arrangement in which a framework stores design data into a common database with an incremental compiler (see, inter alia, Yamagishi section 2.3). This incremental compiler allows for step-wise verification of a logic level circuit to be synthesized prior to completion.

In contrast, the claimed subject matter relates to the modification of signal parameters and automatically updating a pre-existing logic design. ExpressiveSystems is simply illustrating the initial design of a logic design which uses a graphical interface as opposed to a text editor. There is no suggestion that such a logic design may be updated in response to a modification of signal parameters as claimed. Yamagishi describes incremental compilation to simulate incomplete designs without reference to automatically updating design logic.

Therefore, neither of ExpressiveSystems and Yamagishi teach or otherwise suggest the claimed subject matter.

Accordingly, claims 1-25 should be allowable.

Concluding Comments

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Attorney's Docket No.:10559-602001/P12886

Applicant asks that all claims be allowed. Please apply $120 for the Petition for Extension of Time fee and any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 8/8/05

Scott C. Harris
Reg. No. 32,030
Attorney for Intel Corporation

Fish & Richardson P.C.
12390 El Camino Real
San Diego, California 92130
(858) 678-5070 telephone
(858) 678-5099 facsimile

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